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Question Paper Code : X 67558

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electronics and Communication Engineering
EC 1203 – ELECTRONIC CIRCUITS – I
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Identify the components that constitute the dc load in a BJT bias circuit.
2. List the common errors involved in constructing and testing a transistor bias circuit.
3. Compare the performance of CE, CB, CC amplifiers with respect to voltage and current gain.
4. State Miller's theorem.
5. For the given network determine the cut off frequency.

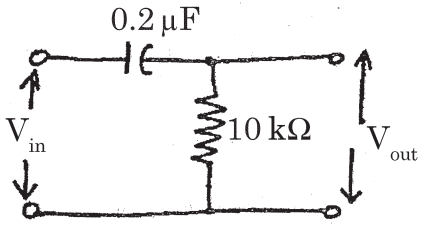


Fig. Q. 5

6. Define Rise Time and Sag of an amplifier.
7. What is the maximum conversion efficiency of class A power amplifier.
8. Draw the circuit of Class-S amplifier.
9. Distinguish between voltage and current feedback connection.
10. What is the effect of negative feedback on gain and bandwidth ?

PART – B **(5×16=80 Marks)**

11. a) i) Draw a circuit of CE transistor amplifier using emitter biasing. Describe qualitatively the stability action of the circuit. **(8)**

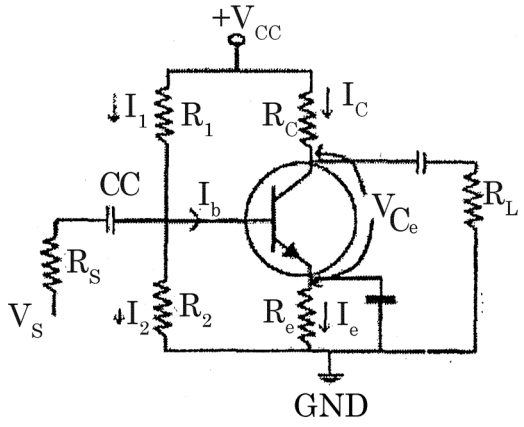
ii) Determine the quiescent currents and the collector to emitter voltage for a silicon transistor with $\beta = 50$ in a self biasing arrangement. Given $V_{CC} = 20$ V, $R_C = 2$ kΩ, $R_e = 0.1$ kΩ, $R_1 = 100$ kΩ, $R_2 = 5$ kΩ. Find the stability factor 'S'. **(8)**

(OR)

b) i) Describe with graphical analysis the fixing of dc operating point. Why is the 'Q' point at the centre of the active region more suitable ? **(8)**

ii) Explain with a neat diagram the voltage divider bias for FET. **(8)**

12. a) Consider a single stage CE amplifier with $R_s = 1$ kΩ, $R_1 = 50$ kΩ, $R_2 = R_E = R_C = 2$ kΩ, $R_L = 2$ kΩ, $h_{fe} = 50$, $h_{ie} = 1.1$ kΩ, $h_{oe} = 25$ μA/V and $h_{re} = 2.5 \times 10^{-4}$. Find A_i, R_i, A_v, A_{vs}, A_{is} and R_0. Use approximate analysis if permissible. **(16)**



(OR)

b) Explain the function of differential amplifier with neat circuit. Derive its A_d, A_c and CMRR. **(16)**

13. a) Determine low cutoff frequency for the network of Fig. Q. (13) (a) using following parameters : $C_s = 10\ \mu F$, $C_E = 20\ \mu F$, $C_c = 1\ \mu F$, $R_s = 1\ k\Omega$, $R_1 = 40\ k\Omega$, $R_2 = 10\ k\Omega$, $R_E = 2\ k\Omega$, $R_C = 4\ k\Omega$, $R_L = 2.2\ k\Omega$, $\beta = 100$, $r_0 = \infty\Omega$, $V_{CC} = 20$ V. **(16)**

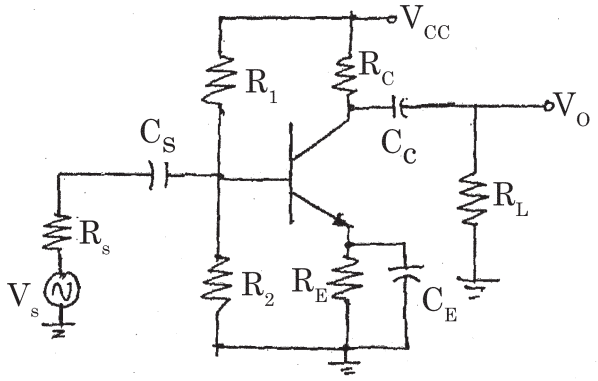


Fig. Q(13)(a)

(OR)

b) Draw the equivalent circuit of source follower at high frequencies and derive expressions for voltage gain, Input Admittance and output Admittance. **(16)**

14. a) i) With neat circuit diagram explain transformer coupled class A Audio power amplifier. **(8)**

ii) Determine the efficiency of class A amplifier. **(8)**

(OR)

b) i) With neat circuit diagram explain class B push pull amplifier. **(8)**

ii) What are the different types of distortion in amplifiers ? Explain. **(8)**

15. a) Draw a sketch and illustrate the principle of series voltage negative feed back and list the major effects of negative feed back on amplifier. **(16)**

(OR)

b) Using illustrations explain the effects of negative feed back on the bandwidth of an amplifier and discuss the effects of open loop gain reduction and closed loop gain. **(16)**